Product Change Notice (PCN)

Date: 7/3/2024

PCN Number: PCN-0331036R-01

To Our Customers:
We appreciate your use of our products. Our commitment in maintaining and improving processes is demonstrated by plans to enhance our product quality, reliability, and manufacturability. The purpose of this notice is to inform you of a product change.

Product(s) Affected: *CMM-4737DT-26186-TR & CMM-4737DT-26386-TR*

Reason(s) for Change: *Updated chip design circuit*

Description of Change: *Detail current consumption lowered to .75mA, signal to noise ratio reduced to 5, power supply reduction updated to -90dBFS. Digital interface changed, as shown below.*
Previous:

parameter	conditions/description	min	typ	max	units
sleep current (I_{SLEEP})	F_{CLOCK} < 1 kHz		25	50	µA
fall-asleep time	F_{CLOCK} < 1 kHz			10	ms
wake-up time	F_{CLOCK} ≥ 1 MHz			10	ms
short circuit current (I_{SC})	grounded data pin		1	10	mA
output load (C_{LOAD})				100	pF
data format	1-Bit PDM				
clock frequency (F_{CLOCK})		1.0	2.4	3.2	MHz
clock duty cycle (F_{DC})		40		60	%
clock rise time (t_{CR})				10	ns
clock fall time (t_{CF})				10	ns
logic input/output low (V_{IOL})	I_{OUT} = 1 mA	-0.30		0.35xV_{DD}	V
logig input/output high (V_{IOH})	I_{OUT} = 1 mA	0.65xV_{DD}		V_{DD}+0.3	V
delay time for valid data (t_{DV})		18		60	ns
delay time for high z (t_{DH})		0		16	ns

Notes: 1. All specifications measured at 23±2°C, humidity at 55±20%, V_{DD} = 2.0 V, F_{CLOCK} = 2.4 MHz, unless otherwise noted.

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New:

parameter	conditions/description	min	typ	max	units
sleep current (I_{SLEEP})	F_{CLOCK} < 1 kHz		3	4	µA
fall-asleep time	F_{CLOCK} < 1 kHz			50	µs
wake-up time	F_{CLOCK} ≥ 1.024 MHz			52	ms
short circuit current (I_{SC})	grounded data pin		1	10	mA
output load (C_{LOAD})				100	pF
data format	1-Bit PDM				
clock frequency (F_{CLOCK})		1.024	2.4	3.25	MHz
clock duty cycle (F_{DC})		40		60	%
clock rise time (t_{CR})				10	ns
clock fall time (t_{CF})				10	ns
logic input high (V_{IH})	I_{OUT} = 1 mA	0.75xV_{DD}			V
logic input low (V_{IL})	I_{OUT} = 1 mA			0.25xV_{DD}	V
logic output high (V_{OH})	I_{OUT} = 1 mA	0.9xV_{DD}			V
logic output low (V_{OL})	I_{OUT} = 1 mA			0.1xV_{DD}	V
delay time for valid data (t_{DV})		18		40	ns
delay time for high z (t_{DH})		0		15	ns

Notes: 1. All specifications measured at 23±2°C, humidity at 55±20%, V_{DD} = 2.0 V, F_{CLOCK} = 2.4 MHz, unless otherwise noted.

Affected Date Code: *All goods purchased after 6/15/2024*

Product Availability: *All goods purchased after 6/15/2024*

PCN Approval:

Operations/Quality

Product Management

F-723-001 Revision: A